WHAT IS CLAIMED IS:

1. A method, comprising:

receiving a first packet for a buffer in memory;

generating a descriptor indicating a length of the first packet and a buffer address of the buffer;

receiving at least one subsequent packet following the first packet capable of fitting in the buffer with the first packet;

generating a descriptor for each received subsequent packet;

transferring to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer; and

adding the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

2. The method of claim 1, wherein in response to receiving one subsequent packet, further performing:

determining whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and

waiting to receive at least one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer if the buffer has available space.

3. The method of claim 1, wherein the buffer comprises a current buffer, wherein in response to receiving one recent subsequent packet, further performing:

determining whether the current buffer has available space for the first packet and the at least one subsequent packet including the recent subsequent packet received before transferring to the current buffer, wherein the first packet and at least one subsequent packet received between the first packet and the recent subsequent packet are transferred in response to determining that that the current buffer does not have available space for the recent subsequent packet, and wherein the descriptor generated for the recent subsequent packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the current

buffer for the recent subsequent packet, and wherein the recent subsequent packet becomes the first packet for the next available buffer.

4. The method of claim 1, wherein the first packets and received subsequent packets are transferred to the buffer in response to a timer expiring.

5. The method of claim 1, wherein all packets in at least one buffer are processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

6. The method of claim 1, wherein the descriptor generated for each subsequent packet that fits into the buffer with the first packet indicates a length of the subsequent packet.

7. The method of claim 1, further comprising:

indicating in the descriptor for the first packet a number of packets included in the buffer, including the first packet and at least one subsequent packet that are transferred to the buffer with the first packet.

8. The method of claim 1, wherein writing the first packet and each subsequent packet comprises transmitting on a bus the first packet and each subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

9. The method of claim 1, wherein the buffer resides in a host memory, wherein an adapter coupled to the host performs receiving the packets, generating the descriptors, transferring the packets to the buffer, and adding the descriptors to a descriptor array.

10. A method, comprising:

accessing a first descriptor referencing a first packet in a buffer and indicating a number of packets in the buffer;

extracting a first packet from the buffer identified in the first descriptor;

accessing at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and

using each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

11. The method of claim 1, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.

12. A system, comprising:

a memory including a plurality of buffers;

an Input/Output (I/O) device interface in data communication with the memory and having circuitry enabled to:

(i) receive a first packet for a buffer in the memory;

(ii) generate a descriptor indicating a length of the first packet and a buffer address of the buffer;

(iii) receive at least one subsequent packet following the first packet capable of fitting in the buffer with the first packet;

(iv) generate a descriptor for each received subsequent packet;

(v) transfer to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer; and

(vi) add the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

13. The system of claim 12, wherein in response to receiving one subsequent packet, the circuitry is further enabled to:

determine whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and

wait to receive at least one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer if the buffer has available space.

14. The system of claim 12, wherein the buffer comprises a current buffer, wherein in response to receiving one recent subsequent packet, wherein the circuitry is further enabled to:

determine whether the current buffer has available space for the first packet and the at least one subsequent packet including the recent subsequent packet received before transferring to the current buffer, wherein the first packet and at least one subsequent packet received between the first packet and the recent subsequent packet are transferred in response to determining that that the current buffer does not have available space for the recent subsequent packet, and wherein the descriptor generated for the recent subsequent packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the current buffer for the recent subsequent packet, and wherein the recent subsequent packet becomes the first packet for the next available buffer.

15. The system of claim 12, further comprising:

a timer, wherein the first packets and received subsequent packets are transferred to the buffer in response to a timer expiring.

16. The system of claim 12, further comprising:

a plurality of processors, wherein all packets in one buffer are processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

17. The system of claim 12, wherein the descriptor generated for each subsequent packet that fits into the buffer with the first packet indicates a length of the subsequent packet.

18. The system of claim 12, wherein the circuitry is further capable of performing:

indicating in the descriptor for the first packet a number of packets included in the buffer, including the first packet and at least one subsequent packet that are transferred to the buffer with the first packet.

19. The system of claim 12, further comprising:

a bus interfacing the memory and the I/O device interface, wherein the circuitry writes the first packet and each subsequent packet by transmitting on the bus the first packet and each subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

20. The method of claim 1, wherein the I/O device comprises a network adapter.

21. A system, comprising:

a memory including a plurality of buffers;

circuitry in data communication with the memory enabled to:

(i) access a first descriptor referencing a first packet in a buffer in the memory and indicating a number of packets in the buffer;

(ii) extract a first packet from the buffer identified in the first descriptor;

(iii) access at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and

(iv) use each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

22. The system of claim 21, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.

23. A system in communication with a network, comprising:

a memory including a plurality of buffers;

an adapter in data communication with the network and the memory and having circuitry enabled to:

(i) receive a first packet for a buffer in the memory;

(ii) generate a descriptor indicating a length of the first packet and a buffer address of the buffer;

(iii) receive at least one subsequent packet following the first packet capable of fitting in the buffer with the first packet;

(iv) generate a descriptor for each received subsequent packet;

(v) transfer to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer; and

(vi) add the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

24. The system of claim 23, wherein in response to receiving one subsequent packet, the circuitry is further enabled to:

determine whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and

wait to receive at least one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer if the buffer has available space.

25. An article of manufacture enabled to cause operations to:

receive a first packet for a buffer in memory;

generate a descriptor indicating a length of the first packet and a buffer address of the buffer;

receive at least one subsequent packet following the first packet capable of fitting in the buffer with the first packet;

generate a descriptor for each received subsequent packet;

transfer to the buffer the first packet and the at least one subsequent packet capable of fitting into the buffer; and

add the descriptors of the first packet and the at least one subsequent packet written to the buffer to a descriptor array.

26. The article of manufacture of claim 25, wherein the operations further comprise in response to receiving one subsequent packet:

determine whether the buffer has available space for the first packet and the at least one subsequent packet received before transferring to the buffer; and

wait to receive at least one more subsequent packet before transferring the first packet and the received at least one subsequent packet capable of fitting into the buffer if the buffer has available space.

27. The article of manufacture of claim 25, wherein the buffer comprises a current buffer, wherein the operations further comprise in response to receiving one subsequent packet:

determine whether the buffer has available space for the first packet and the at least one subsequent packet including the recent subsequent packet received before transferring to the buffer, wherein the first packet and at least one subsequent packet received between the first packet and the recent subsequent packet are transferred in response to determining that that buffer does not have available space for the recent subsequent packet, and wherein the descriptor generated for the recent subsequent packet indicates a next buffer address of a next available buffer in the memory in response to determining that there is not enough available space in the buffer for the recent subsequent packet, and wherein the recent subsequent packet becomes the first packet for the next available buffer.

28. The article of manufacture of claim 25, wherein the first packets and received subsequent packets are transferred to the buffer in response to a timer expiring.

29. The article of manufacture of claim 25, wherein all packets in at least one buffer are processed by one processor and wherein packets in different buffers are capable of being processed by different processors.

30. The article of manufacture of claim 25, wherein the descriptor generated for each subsequent packet that fits into the buffer with the first packet indicates a length of the subsequent packet.

31. The article of manufacture of claim 25, wherein the operations further comprise:

indicate in the descriptor for the first packet a number of packets included in the buffer, including the first packet and at least one subsequent packets that are transferred to the buffer with the first packet.

32. The article of manufacture of claim 25, wherein writing the first packet and each subsequent packet comprises transmitting on a bus the first packet and each subsequent packet capable of fitting into the buffer in a single bus transaction to the buffer.

33. The article of manufacture of claim 25, wherein the buffer resides in a host memory, wherein an adapter coupled to the host performs receiving the packets, generating the descriptors, transferring the packets to the buffer, and adding the descriptors to a descriptor array.

34. An article of manufacture enabled to cause operations to:

access a first descriptor referencing a first packet in a buffer and indicating a number of packets in the buffer;

extract a first packet from the buffer identified in the first descriptor;

access at least one subsequent descriptor, where the accessed subsequent descriptor is associated with one subsequent packet indicated in the number of packets, and wherein the subsequent descriptor indicates a length of the associated subsequent packet; and

use each accessed subsequent descriptor to access the associated subsequent packets in the buffer.

35. The article of manufacture of claim 34, wherein the packets are transmitted over a network to an adapter, wherein the adapter generates the descriptors and transfers the packets to buffers in a host memory, and wherein an adapter driver uses the descriptors to access one or more packets from the buffers in the host memory in response to receiving a signal from the adapter that packets are in the host memory.